

7A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

The 7N50 is an N-channel mode power MOSFET using an advanced technology to provide customers with planar stripe. The technology reduces the conduction loss, improves switching performance and enhances the avalanche energy.

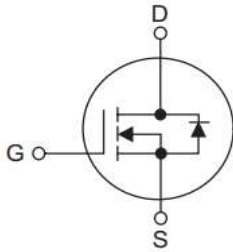
This power MOSFET is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

FEATURES

- * $R_{DS(ON)} < 1.0\Omega @ V_{GS}=10V, I_D=3.5A$
- * Fast Switching Capability
- * 100% avalanche tested

SYMBOL

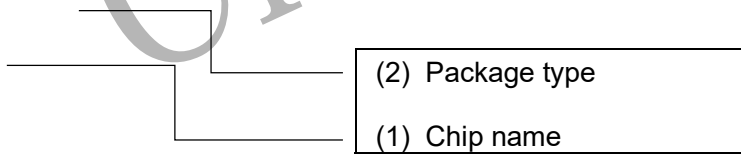
1. Gate
2. Drain
3. Source



Package Description

Product Model	Package Type	Mark Name	Identification Code	Package
CMN7N50F	TO-220F	CMN7N50	F	Tube

CMN7N50 F



(1) CMN7N50: 500V 7A (2) F:TO-220F

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous ($T_C=25^\circ\text{C}$)	I_D	7	A
	Pulsed (Note 2)	I_{DM}	28	A
Avalanche Current (Note 3)		I_{AR}	5.5	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	151	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.7	V/ns
Power Dissipation	$T_C=25^\circ\text{C}$ TO-220F	PD	48	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes:

- Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
- Repetitive Rating: Pulse width limited by maximum junction temperature
- $L = 10\text{mH}$, $I_{AS} = 5.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- $I_{SD} \leq 7.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	PACKAGE	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	TO-220F	2.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	TO-220F	62.5	$^\circ\text{C}/\text{W}$

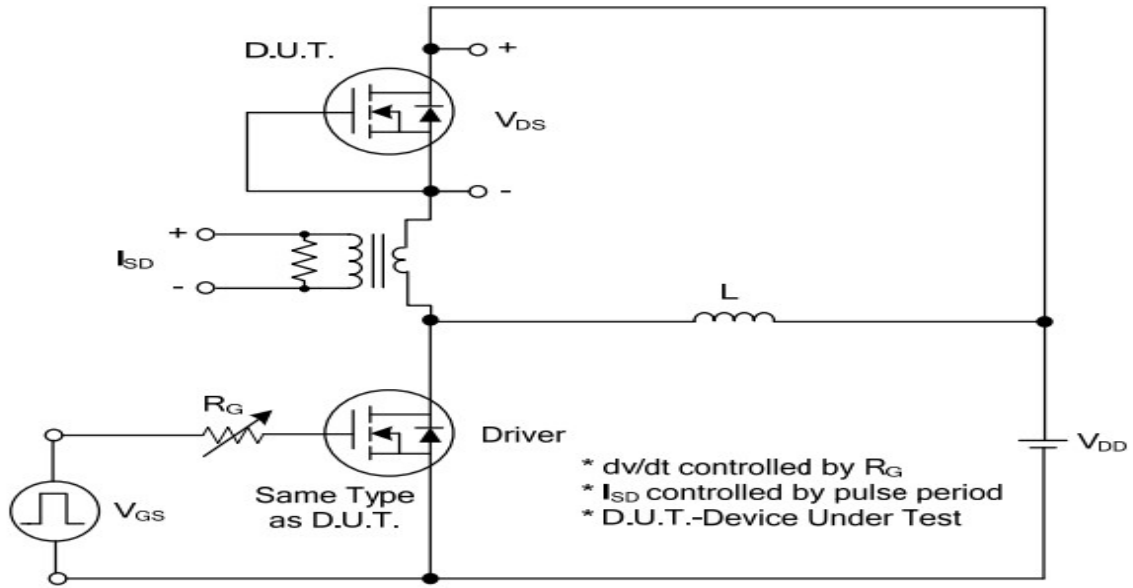
ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 500\text{V}$, $V_{GS} = 0\text{V}$			1	μA
Gate- Source Leakage Current	Forward	$V_{GS} = +30\text{V}$, $V_{DS} = 0\text{V}$			+100	nA
	Reverse	$V_{GS} = -30\text{V}$, $V_{DS} = 0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{V}$, $I_D = 3.5\text{A}$		0.8	0.9	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$		1000		pF
Output Capacitance	C_{OSS}			95		pF
Reverse Transfer Capacitance	C_{RSS}			75		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS} = 10\text{V}$, $V_{DS} = 50\text{V}$, $I_D = 1.3\text{A}$ $I_G = 100\mu\text{A}$ (Note 1, 2)		65		nC
Gate to Source Charge	Q_{GS}			5.8		nC
Gate to Drain Charge	Q_{GD}			6.0		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 0.5\text{A}$, $R_G = 25\Omega$ (Note 1, 2)		53		ns
Rise Time	t_R			36		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			160		ns
Fall-Time	t_F			38		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				7	A
Maximum Body-Diode Pulsed Current	I_{SM}				28	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S = 7\text{A}$, $V_{GS} = 0\text{V}$			1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$I_S = 7\text{A}$, $V_{GS} = 0\text{V}$, $di_F/dt = 100\text{A}/\mu\text{s}$ (Note 1)		245		ns
Body Diode Reverse Recovery Charge	Q_{RR}				1.45	

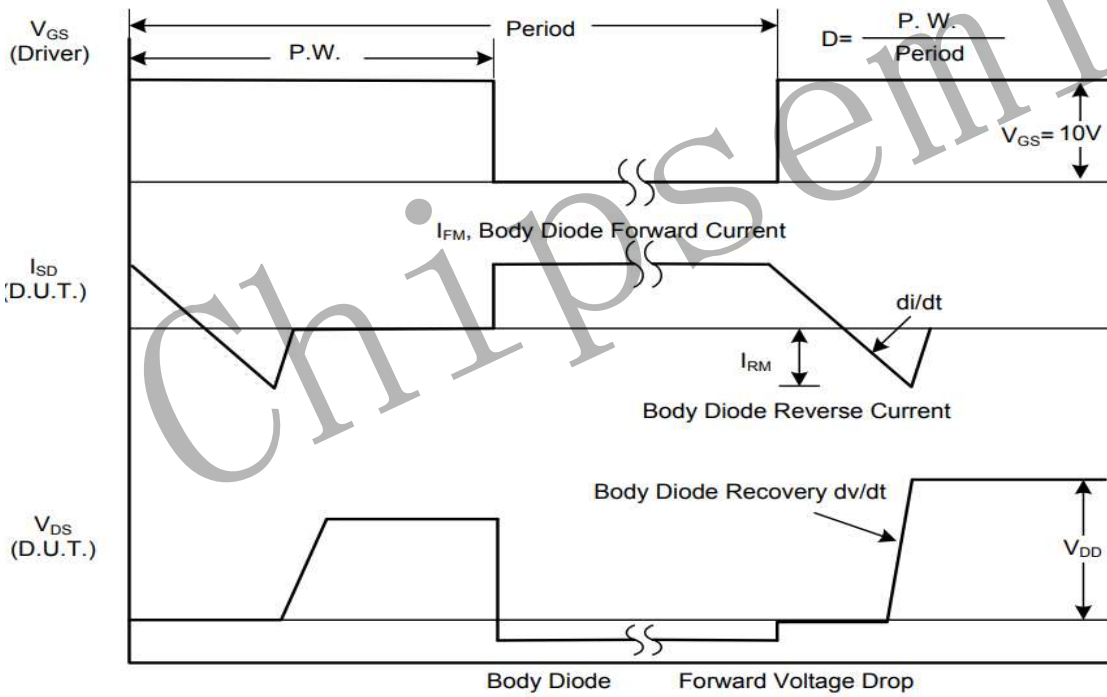
Notes:

1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.
2. Essentially independent of operating temperature.

TEST CIRCUITS AND WAVEFORMS

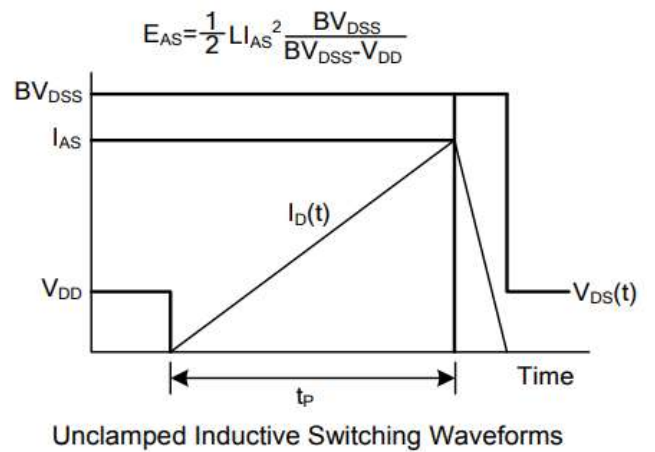
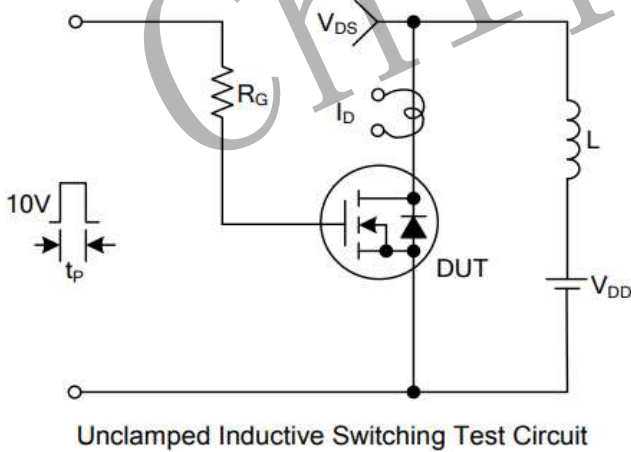
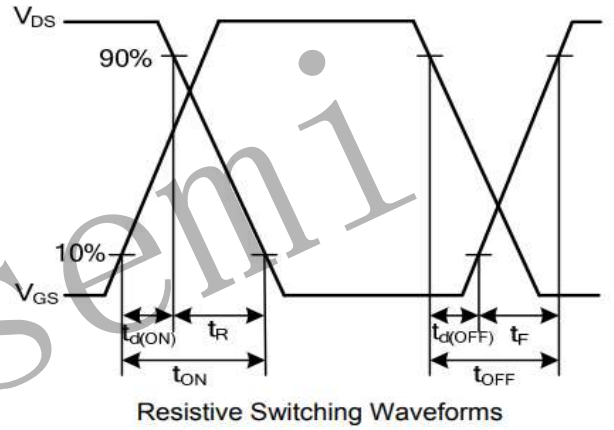
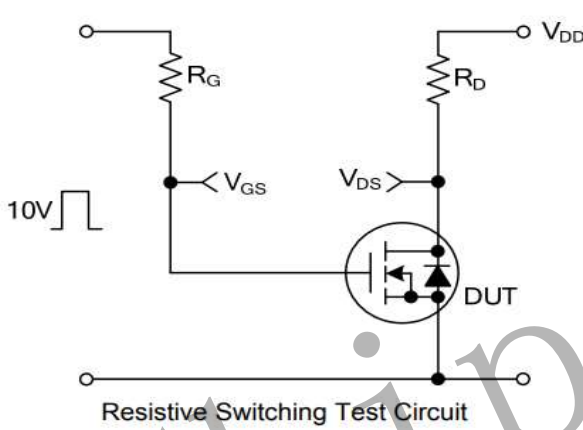
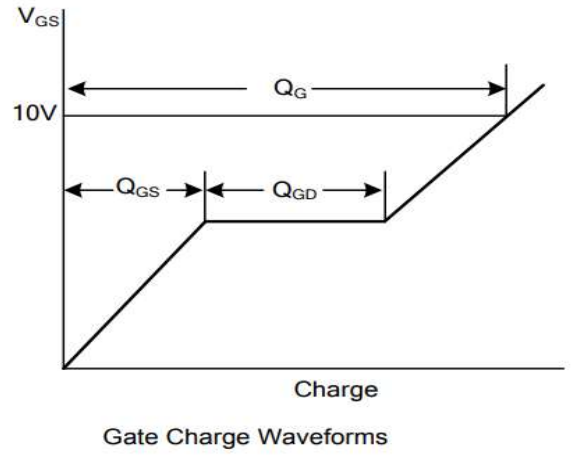
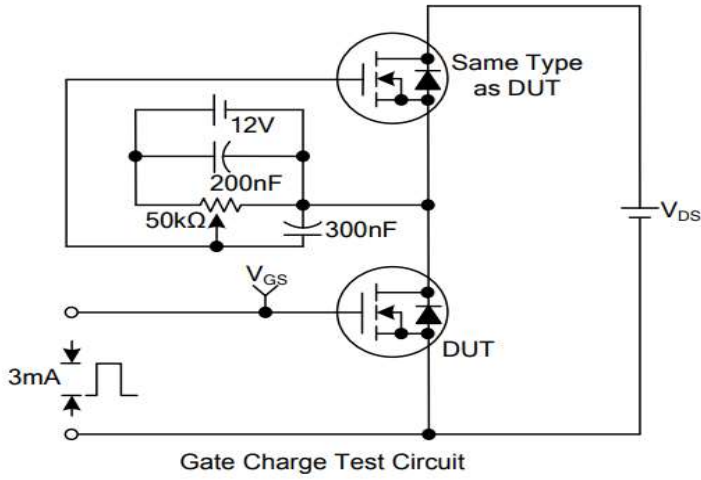


Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

TEST CIRCUITS AND WAVEFORMS(Cont.)



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Attentions

- Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
- When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
- MOSFET is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
- Chipsemi reserves the right to make changes in this specification sheet and is subject to change without prior notice.

Appendix

Revision history:

Date	REV.	Description	Page
2023.3	1.0	Original	6

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