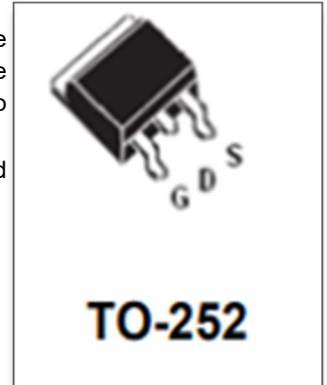


5A, 550V N-CHANNEL POWER MOSFET

DESCRIPTION

The **5N50** is an N-channel power MOSFET adopting CMD's advanced technology to provide customers with DMOS, planar stripe technology. This technology is designed to meet the requirements of the minimum on-state resistance and perfect switching performance. It also can withstand high energy pulse in the avalanche and communication mode.

It can be used in applications, such as active power factor correction, high efficiency switched mode power supplies, electronic lamp ballasts based on half bridge topology.

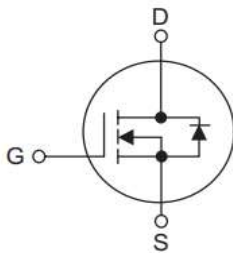


FEATURES

- * $R_{DS(ON)} < 1.4\Omega$ @ $V_{GS} = 10V, I_D = 2.5A$
- * 100% avalanche tested
- * High switching speed

SYMBOL

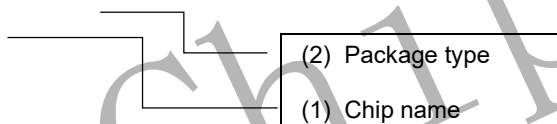
1. Gate
2. Drain
3. Source



Package Description

Product Model	PackageType	Mark Name	Identification Code	Package
CMN5N50D	TO-252	CMN5N50	D	Tape Reel

CMN5N50D



(1) CMN5N50: 500V 5A

(2) D:TO-252

ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	10	A
Avalanche Current (Note 2)		I_{AR}	5	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	133	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.25	V/ns
Power Dissipation	$T_c=25^\circ\text{C}$ TO-252	P_D	54	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^\circ\text{C}$

Notes:

- Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
- Repetitive Rating: Pulse width limited by maximum junction temperature
- $L = 10\text{mH}$, $I_{AS} = 5.15\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- $I_{SD} \leq 5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	PACKAGE	RATINGS	Units
$R_{\theta JC}$	Junction-to-Case	TO-252	2.13	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	TO-252	110	$^\circ\text{C}/\text{W}$

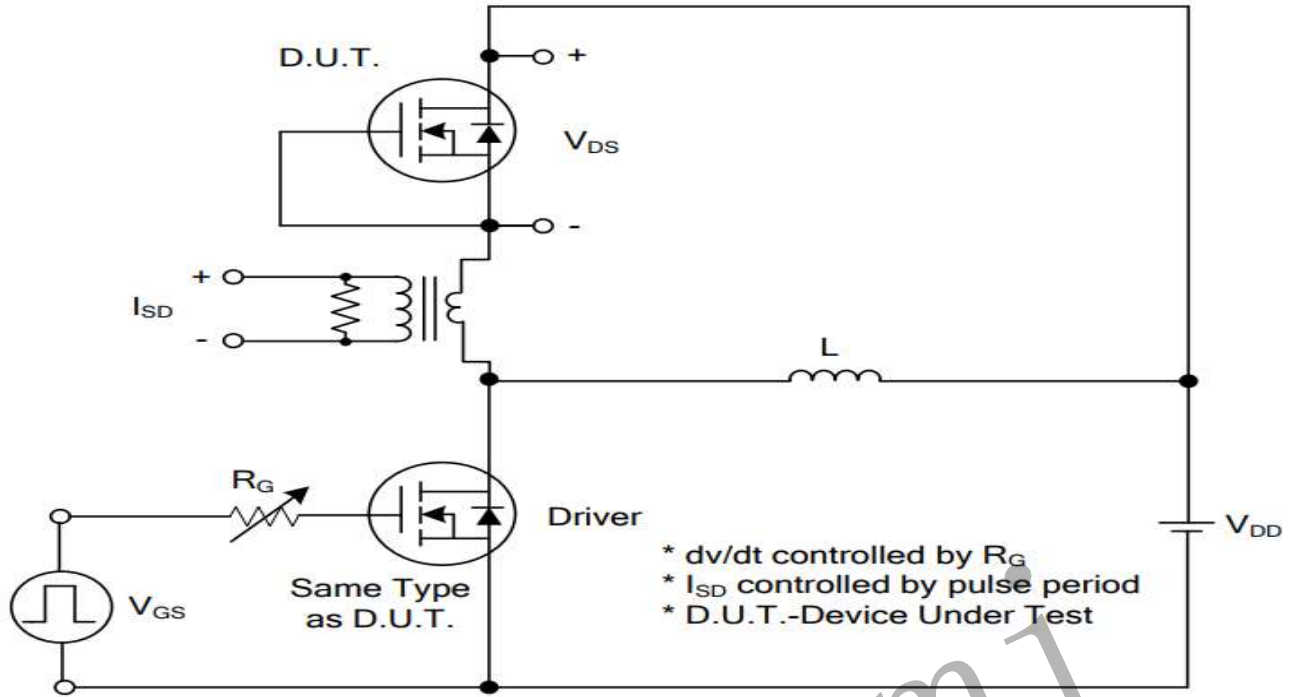
ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate- Source Leakage Current	Forward	I_{GSS}			100	nA
	Reverse					
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=2.5\text{A}$			1.4	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		438		pF
Output Capacitance	C_{OSS}			61		pF
Reverse Transfer Capacitance	C_{RSS}			4.6		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=5.0\text{A}$, $R_G=25\Omega$ (Note 1, 2)		7		ns
Rise Time	t_R			18		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			32		ns
Fall-Time	t_F			20		ns
Total Gate Charge	Q_G			13		nC
Gate to Source Charge	Q_{GS}			5.5		nC
Gate to Drain Charge	Q_{GD}	$I_D=5.0\text{A}$, $I_G=100\mu\text{A}$ (Note 1, 2)		2		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				5	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				10	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Charge	Q_{RR}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$, $dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		250		ns
				1.78		μC

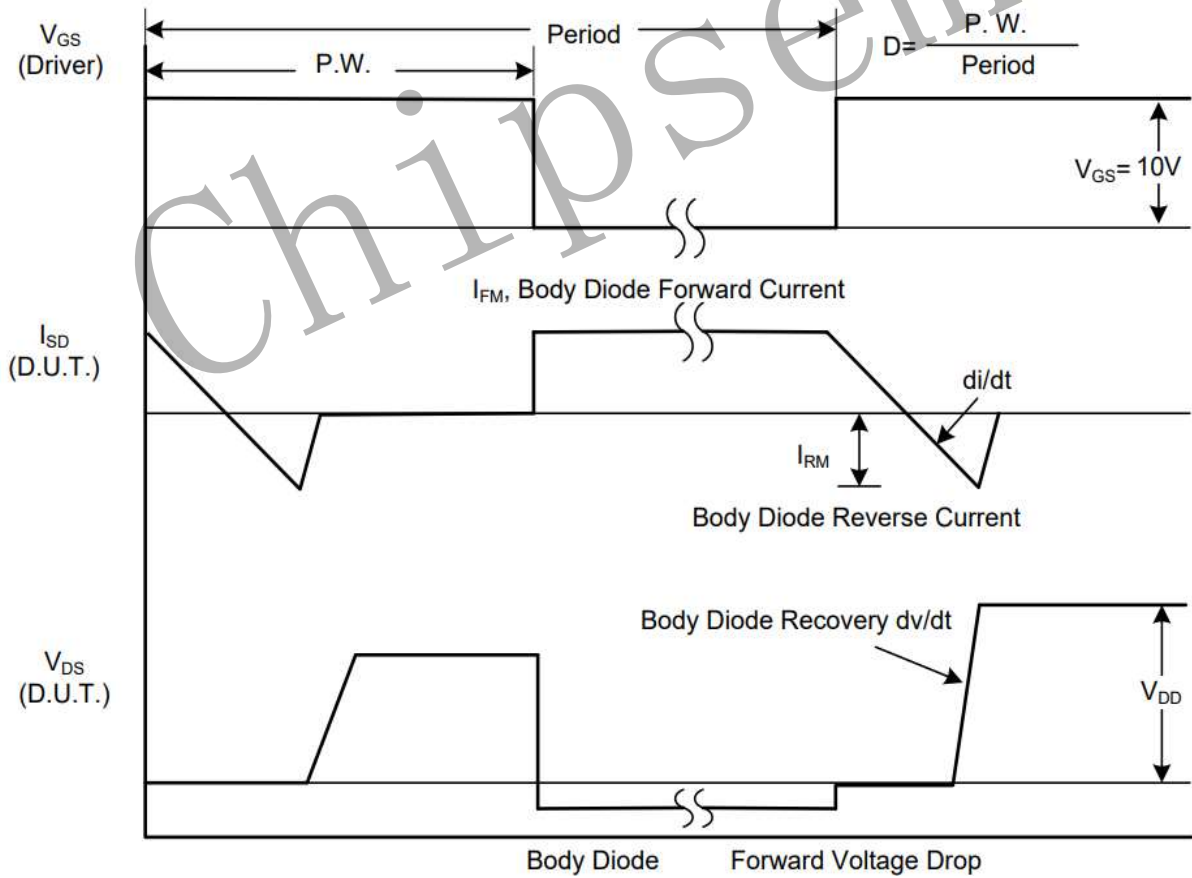
Notes:

1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperatur

TEST CIRCUITS AND WAVEFORMS

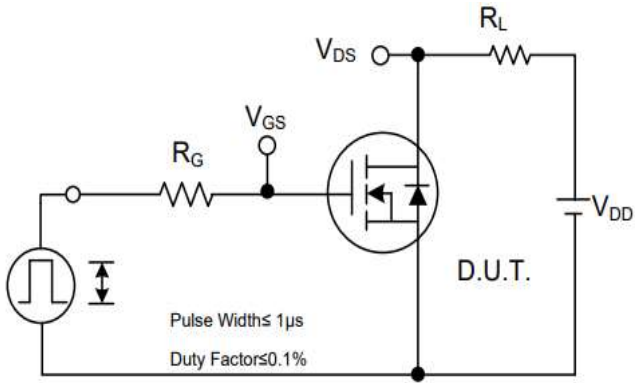


Peak Diode Recovery dv/dt Test Circuit

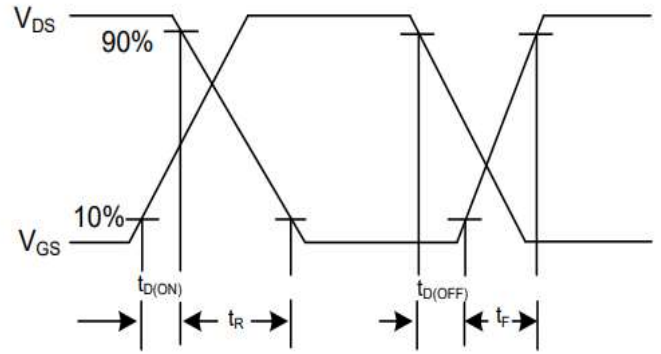


Peak Diode Recovery dv/dt Waveforms

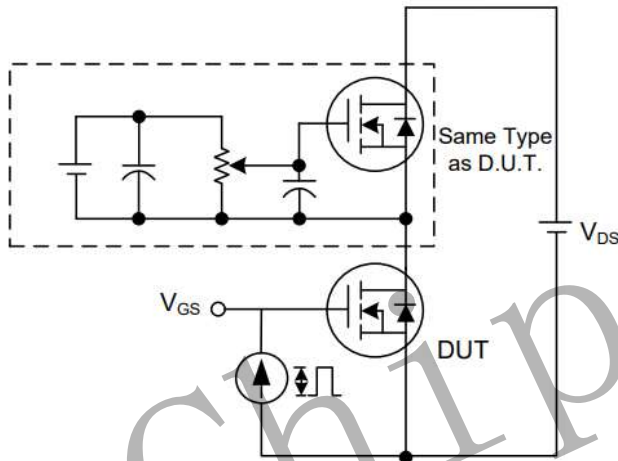
TEST CIRCUITS AND WAVEFORMS



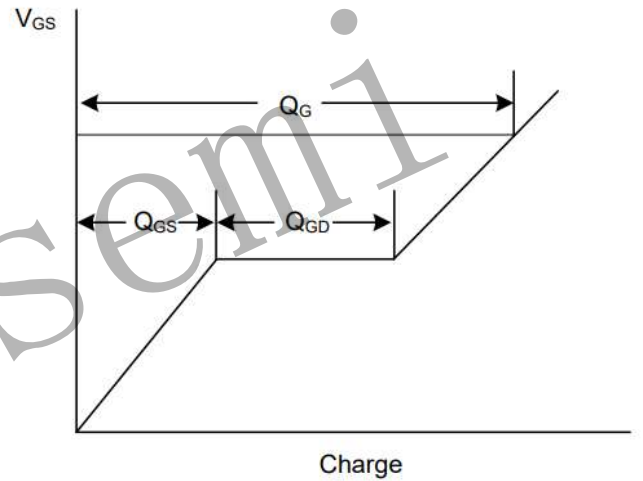
Switching Test Circuit



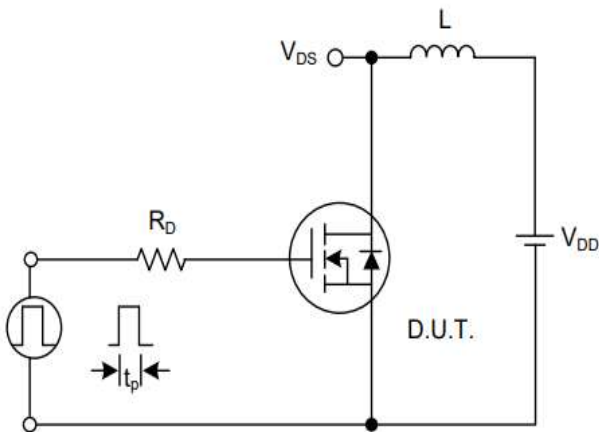
Switching Waveforms



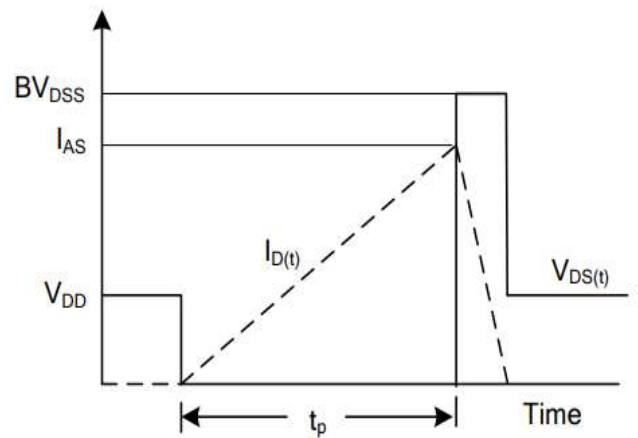
Gate Charge Test Circuit



Gate Charge Waveform

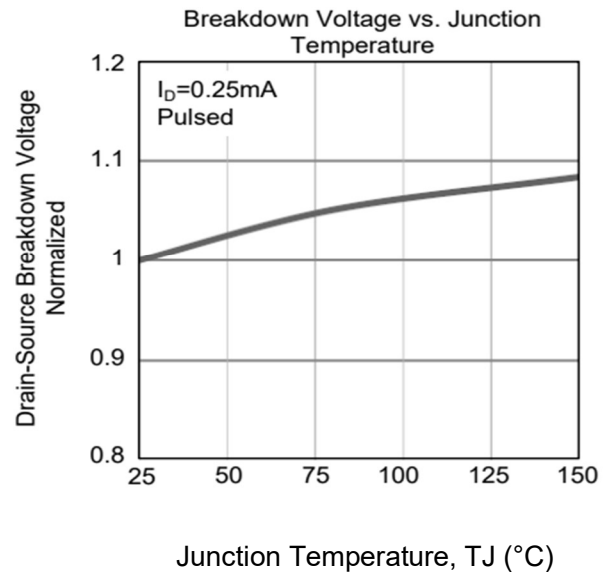
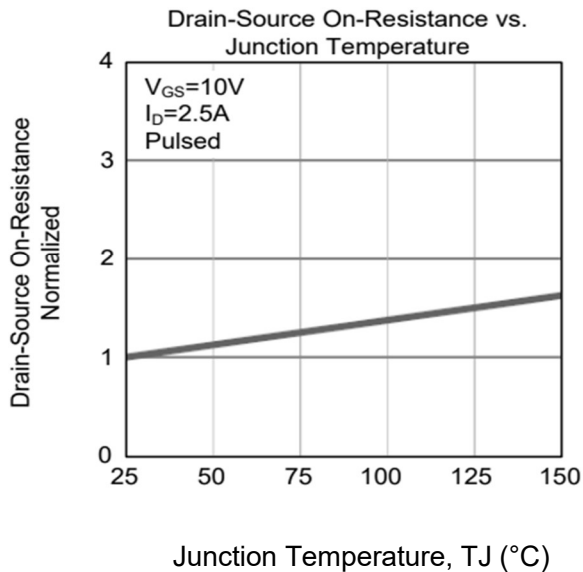
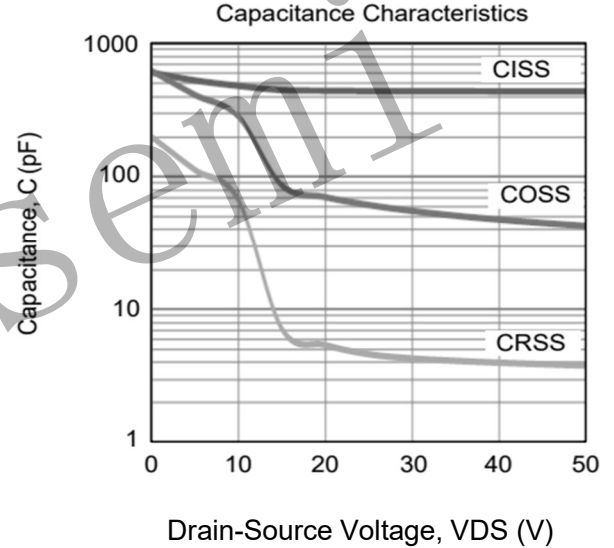
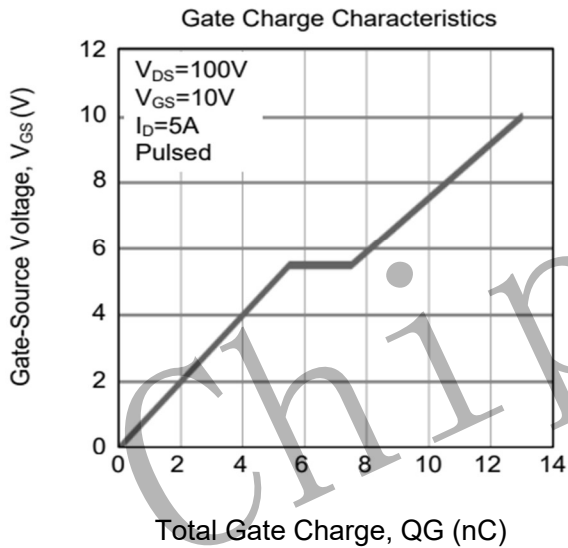
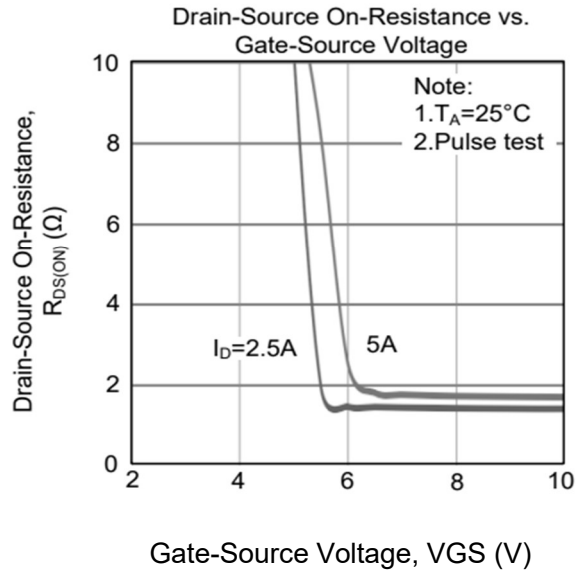
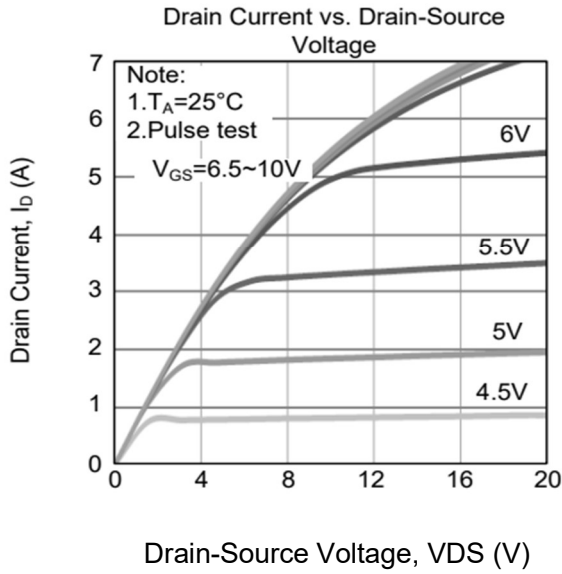


Unclamped Inductive Switching Test Circuit

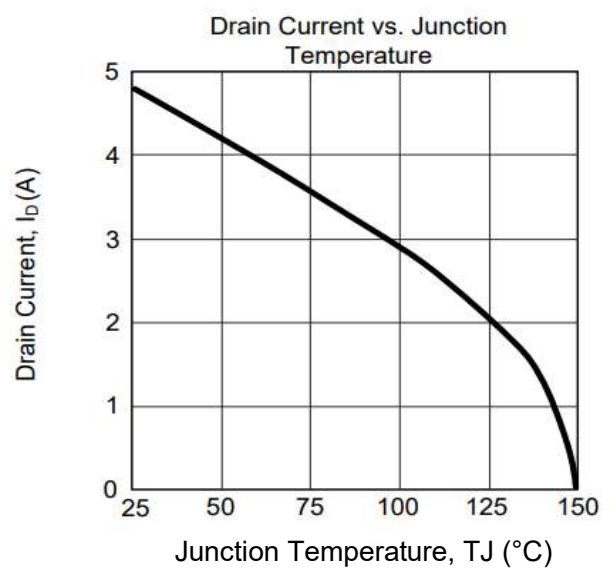
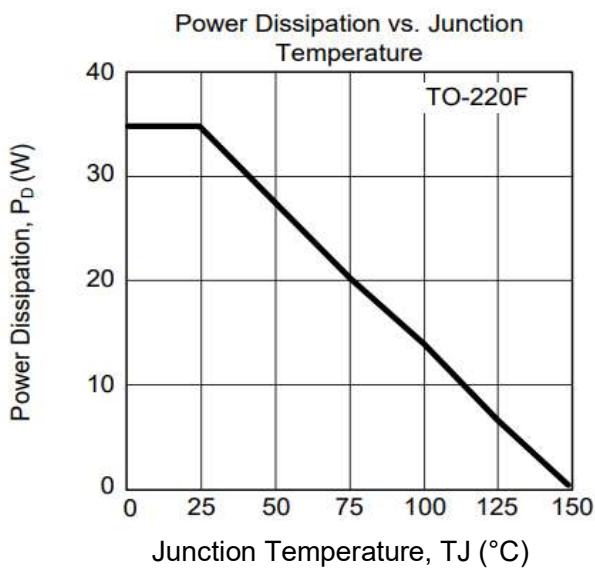
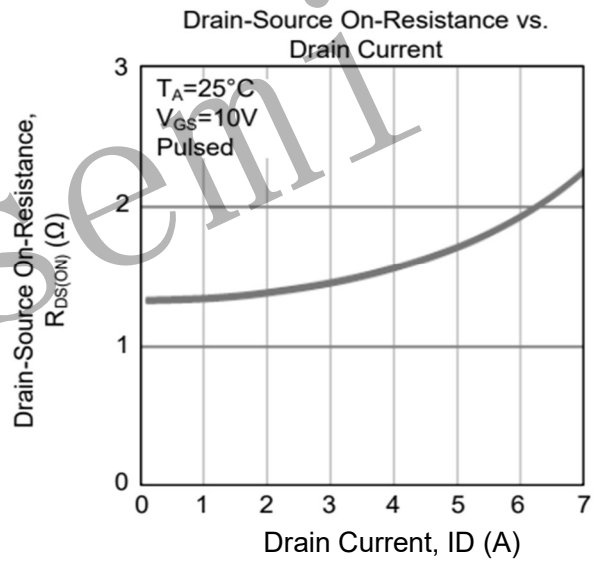
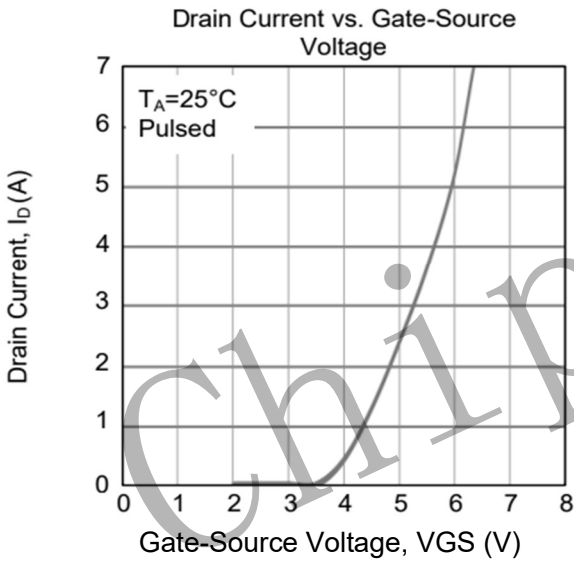
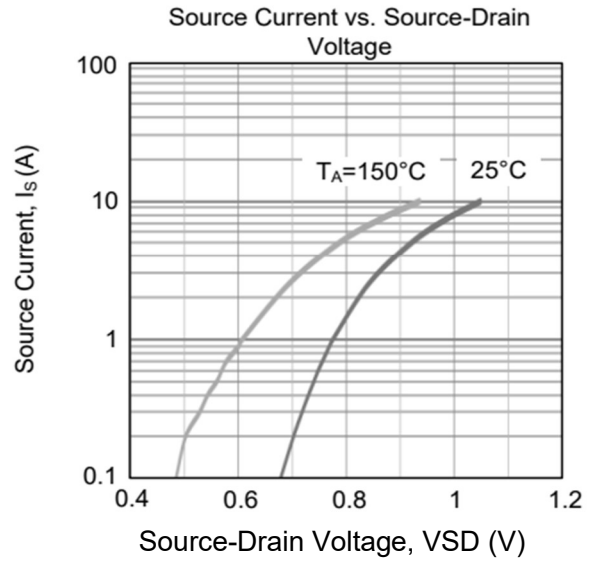
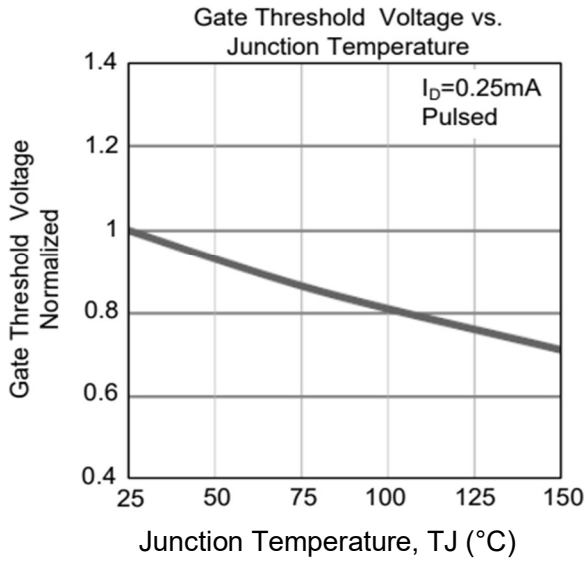


Unclamped Inductive Switching Waveforms

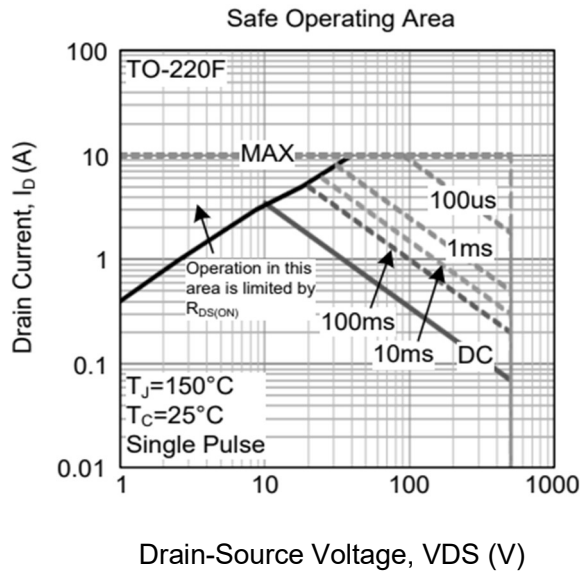
YPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (Cont.)



TYPICAL CHARACTERISTICS (Cont.)



Attentions

- Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
- When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
- MOSFET is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
- Chipsemi reserves the right to make changes in this specification sheet and is subject to change without prior notice.

Appendix

Revision history:

Date	REV.	Description	Page
2023.3	1.0	Original	8